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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

INFINEON TECHNOLOGIES AG,

Plaintiff,

vs.

VOLTERRA SEMICONDUCTOR CORPORATION,

Defendant.

Case No. CV-11-6239 (MMC)

VOLTERRA'S CORRECTED RESPONSIVE CLAIM CONSTRUCTION BRIEF

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Pursuant to the Court's September 13, 2013 Case Management Order, Volterra submits this Responsive Claim Construction Brief relating to United States Patent No. 5,945,730 (the "'730 Patent" or the "Sicard Patent").

I. INTRODUCTION

It is fundamental that the proper scope of a patent claim must be grounded in an understanding of "what the inventors actually invented and intended to envelop with the claim." *Phillips v. AWH Corp*., 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc). Consistent with that principle—and the law governing claim construction—Volterra proposes constructions that fully encompass, but do not unfairly exceed, the boundaries of the semiconductor power device that the '730 patent discloses and claims, as understood by a person of ordinary skill in the art.

In contrast, Infineon's proposed claim constructions repeatedly ignore this guidance, and instead reflect an attempt to (1) use this case as a vehicle to relitigate key disputes about the Sicard Patent that were previously decided by Judge Spero in a related litigation between the parties involving the same patent, (2) obscure or side-step the actual dispute for each term, and (3) ignore the express language of the claims and consistent description in the context of the claimed invention to stretch the Sicard Patent to cover disclaimed technology that would run contrary to the stated goals of the patent.

In a number of instances, Infineon's approach is to propose that significant claim limitations that frame core disputes on ultimate issues simply go unconstrued such that Infineon can pursue sweeping infringement theories through summary judgment and trial—the same theories about the Sicard Patent that Infineon fought and lost in front of Judge Spero. Infineon tries to veil this strategy by attacking portions of Volterra's constructions on grounds not only divorced from the specification and the plain language of the claims, but which are irrelevant to the issues in this case.[1] All told, Infineon's constructions fail to give meaning to the true scope of

[1] As Infineon acknowledges throughout its opening brief, "claim construction 'is not an obligatory exercise in redundancy,' but rather is 'a matter of resolution of disputed meanings and technical scope, to **clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement**.'" D.I. 300 [Opening Br.] at 21 (quoting *U.S. Surgical Corp. v. Ethicon Inc.*, 103 F.3d 1554, 1568 (Fed Cir. 1997)); *see also id.* at n. 9.

the invention, or to give effect to the fundamental principle that claims should be construed to cover what was actually invented—no more and no less.

II. LEGAL FRAMEWORK

The Court is familiar with the pertinent claim construction principles. *See* Declaration of Blake Davis In Support Of Volterra's Resp. Claim Construction Brief ("Davis Decl."), Ex. A [*Synopsys* Order] at 2-3. Volterra cites authority on a term-by-term basis in the body of the brief.

III. OVERVIEW OF THE ASSERTED PATENT

For purposes of claim construction, Infineon's overview of the Sicard Patent is generally accurate from a technical perspective. However, Infineon's description does not clearly define the goals of the Sicard Patent and improperly characterizes it as a "packaging patent."

The Sicard Patent is directed to power semiconductor devices. Sicard Patent at 1:1-5, 2:8-12. Power semiconductor devices are chips that handle applications requiring large amounts of electrical current flowing through the device. *Id.* at 1:16-27. One of the problems associated with power semiconductor devices is these devices have a high resistance when they are turned on (the "on-resistance" or "Rdson") which causes high power dissipation because the large amounts of current must travel through thin metal regions (*e.g.*, the final (top) thin metal layer of the power semiconductor device and wire bonds) to reach the external access points of the semiconductor device where it connects to other components within a larger device such as a circuit board that could be used in a server. *Id.* at 1:16-27; *see also* Declaration of Jeffrey D. Baxter in Support of Plaintiff Infineon's Opening Brief (D.I. 301) ("Baxter Decl."), Ex. 3 [Schaper Op. Decl.] ¶ 72. On-resistance is undesirable because it requires a larger area to provide sufficient power dissipation associated with the high currents. *Id.* at 1:19-20. Several prior art solutions had been developed to address the on-resistance associated with high current power semiconductor devices, but they came at the expense of either increasing the size or increasing the cost, complexity and manufacturing time of the device. The Sicard Patent thus purports to reduce the on-resistance to allow the power semiconductor device to handle higher currents without increasing the size of the device at a lower cost and complexity than prior art solutions. *Id.* at 1:23-27; *see id.* at 1:53-58.

The Sicard Patent describes two prior art solutions to reduce the added resistance of the

final metal layer. The first solution uses multiple wire connections (wire bonds) between the metal conductors and the external access points. Sicard Patent at 1:32-37. However, Sicard explains that, due to the "large number of wires," such a solution "considerably increases the size of the power device" and is "extremely expensive" (because each wirebond needed to be created individually, taking significant time). *Id*. at 1:40-44. The second described prior art solution used a "thick copper metal deposited on the die above the final metal conductors" and "large aluminum wires bonded on the semiconductor regions" rather than multiple wirebonds. *Id*. at 1:48-52. However, Sicard criticizes this solution because the "additional deposition step" of the third thick copper layer "increases the complexity and cycle time of the manufacturing process which adds significant cost to the integrated power device." *Id*. at 1:52-55. An object of Sicard is to "provide an improved semiconductor power device which mitigates the above mentioned problems." *Id*. at 1:56-58. Consistent with this objective, Sicard describes its purported invention as one that does not need wirebonds or wire bond pad areas and does not require an expensive third thick metal deposition process as used in the described prior art. *Id*. at 4:67-5:9.

To achieve its stated goals, the purported invention adds a lead frame and bumps connected to the standard metal conductors of a power semiconductor.[2] The lead frame is a highly-conductive thick external metal structure that extends over the semiconductor regions of the power semiconductor device, provides support for the power semiconductor device, and enables the device to be connected to external components or wiring. *See id*. at 3:13-20, 5:4-9. This solution reduces the resistance associated with the final metal layer because the bumps on the metal conductors provide connections that shorten the distance that the current must travel through the thin metal elements (the metal conductors) before flowing off the chip into the thicker metal. *Id.* at 3:49-54, 4:40-45.

IV. LITIGATION HISTORY

Litigation between the parties began in November 2008, soon after Volterra learned Infineon and its affiliates had introduced voltage regulator products that copied Volterra's core IP

[2] As will be addressed in the context of Volterra's invalidity defenses, the purported solutions described and claimed in Sicard were already known in the art.

and infringed Volterra's patents. *Volterra Semiconductor Corporation v. Primarion, Inc. et al.*, Case No. 08-cv-05129 JCS (N.D. Cal.) (hereinafter the "Volterra Action"). In that litigation, Volterra asserted five patents covering integrated power switches, including Volterra's U.S Patent Nos. 6,278,264 and 6,462,522 (together the "Burstein Patents").

The Sicard Patent was initially raised in the Volterra Action (unsuccessfully) as prior art to the Burstein Patents. Infineon subsequently purchased the patent and filed suit in Delaware six days later, while the California action was pending. Volterra successfully moved to transfer this action to this Court, based on its close relationship with the Volterra Action. Once transferred, Infineon refused to consent to Judge Spero for this case, presumably because Judge Spero had already rejected Infineon's arguments as to the scope of the Sicard Patent. Indeed, Judge Spero determined that, contrary to Infineon's urging, the Sicard Patent does not disclose the subject matter of the Burstein Patents, which are embodied in the accused products here.

The crux of the dispute in this case is whether the Sicard Patent can cover a power semiconductor device that uses an interface layer located between the final metal layer and the solder bumps. In the accused products, this interface layer is called an under bump metallization layer (UBM) or redistribution layer (RDL). This issue, however, was already decided on summary judgment in the previous litigation, where Judge Spero held that Sicard "not only fails to disclose, but actually teaches away from using a UBM layer." Davis Decl., Ex. B [Volterra Action Order Re SJ Motions] at 70-71.

There, Judge Spero determined that Infineon did "not challenge [Volterra's expert] Dr. Szepesi's[3] opinion that a person skilled in the art would have understood that **use of a UBM layer**

[3] In its opening brief, Infineon's devotes considerable attention to challenging the credentials of Volterra's expert Dr. Szepesi. *See* D.I. 300 [Opening Br.] at 4-5. But there is no genuine question that Dr. Szepesi is qualified as an expert on the technology at issue. Dr. Szepesi has more than 30 years of experience developing and designing power semiconductor devices. D.I. 301-4, Baxter Decl., Ex. 4 [Szepesi Op. Decl] ¶¶ 5-11. Judge Spero considered and relied on Dr. Szepesi's opinions on the Sicard Patent in the prior litigation, and qualified Dr. Szepesi as an expert in the previous litigation. *See* Davis Decl., Ex. B [Volterra Action Order Re SJ Motions] at 72-75; Davis Decl., Ex. G [2011-05-18 Trial Transcript] at 1215:21-23. Infineon's expert even testified in deposition in this case that "[c]learly, Dr. Szepesi and I – and I think we both understand the technologies involved [in Sicard]." Davis Decl., Ex. C [2014-03-28 Schaper Dep. Tr.] at 102:5-103:7.

would have been inconsistent with an important benefit of Sicard's invention, namely, a semiconductor chip that was easier and less expensive to manufacture than chips in the prior art that required a thick metal deposition process." *Id.* at 72.[4] Undeterred by its previous failure, Infineon comes before this Court to litigate the same issue.

V. ARGUMENT

A. "first metal conductors" and "second metal conductors"[5] (Claims 1-8)

Claim Term	Infineon's Proposed Construction	Volterra's Proposed Construction
"first metal conductors" "second metal conductors"	plain and ordinary meaning	a first part of the final metal layer a second part of the final metal layer

The dispute is whether the claimed first and second metal conductors are part of the final metal layer to which the invention is directed (Volterra's position) or can be any metal that conducts including some sort of interface layer above the final metal layer of the device (Infineon's position). The dispute arises from Infineon's effort to construe the terms divorced from the claimed invention and the knowledge of one skilled in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) ("Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification."); *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) (rejecting an approach that would look at the words of the claim with no context as to what the contested term does and how it works) (*citing DeMarini Sports, Inc. v. Worth*, 239 F.3d 1314, 1324 (Fed. Cir. 2001) ("We cannot look at the ordinary meaning of the term 'frame' in a vacuum.")). Under Infineon's theory, the first and second metal conductors can be any shape, any location within or on the device, and any conceivable "metal that permits an electric current to flow." D.I. 300 [Opening Br.] at 5. However, the first and second metal conductors as used in the asserted claims, and as described in the specification, are part of the final metal layer, which is the metal

[4] Emphasis added and internal citations omitted throughout, unless otherwise noted.

[5] Infineon treats the disputed term as "metal conductors." In fact, the terms to be construed are "first metal conductors" and "second metal conductors." Davis Decl., Ex H [JCCS] at 1-2.

that has the high on-resistance that the Sicard Patent is attempting to address.

1. Volterra's Construction Gives The Claim Appropriate Meaning In View Of The Specification And The Objectives Of The Patent

Looking at the intrinsic record, it is clear that the "first metal conductors" and "second metal conductors" refer to parts of the final metal layer of the chip. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 29. The claims require a "plurality of [first/second] metal conductors" which are "**coupled to the [first/second] semiconductor region**, each of the plurality of [first/second] metal conductors having **at least one bump in contact therewith**." Sicard Patent at Claim 1. Additionally, the "at least one bumps of the [first/second] metal conductors must be accessible outside the die such that they can **connect** to the "[first/second] connection portions" of the "frame." *Id.* at Claim 1. Due to these requirements—that the bumps which are in contact with the first and second metal conductors must also be accessible to connect to the external frame—the metal conductors must be the final metal layer of the device. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 29. Logically, if the metal conductors were part of a lower metal layer, the bumps in contact with the metal conductors would not be externally accessible as other layers would be above them. This is also shown in Sicard, where these different connections are only made by parts of the final metal layer. *Id.*; *see also* Sicard Patent at Figs. 6, 7.

The patent consistently describes the metal conductors as part of the final metal layer (in this case, the second layer) that is created during the fabrication of the semiconductor. For example, Sicard describes the standard LDMOS devices as including "[f]inal metal conductors [that] extend across the drain and source semiconductor regions to connect the semiconductor regions to respective bonding pads." *Id.* at 1:12-15. Sicard's Figs. 1, 2, 4, and 5 are all top plan views showing the first and second conductors in the same layer, which Fig. 6 illustrates as part of the second (final) metal layer. *Id.* at 2:12-17; 2:20-25; 4:20-22, Figs 1, 2, 4, 5; *see id.* at Fig. 6 (element 34). The specification also makes clear that the first and second metal conductors are parts of the final metal layer. For example, the preferred embodiment of Sicard describes a two-layer LDMOS power transistor in which the second layer is deposited above the first metal layer and forms the "metal conductor" of the claims. *Id.* at 4:7-29 ("a second metal layer is deposited

on the second oxide layer 40 to form the metal conductor 34"); *see id*. at Figs. 6, 7. Infineon does not dispute that the only first and second metal conductors disclosed are part of the final metal layer. *See* D.I. 300 [Opening Br.] at 6:20-27. No other metal conductor is described or hinted at as being the claimed first and second metal conductors. *See* D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi Reb. Decl.] ¶¶ 31-33.

Importantly, the patent's requirement that the first and second metal conductors are part of the final metal layer is not merely an embodiment, but the very basis of the purported invention. The invention is described as applicable to devices where the conductors have certain undesirable characteristics as part of the final metal layer (final metal interconnects).

> The present invention will now be described with reference to a LDMOS power transistor device. It will however be appreciated that the **invention can be applied to any power device where the resistance of the final metal influences the current capability of the device**, for example devices having long **final metal interconnects** such as lateral power transistors.

Sicard Patent at 2:36-42. Again, it is the large amounts of current that must flow through these long, thin final layers in power devices that creates the high on-resistance that the bumps and frame in Sicard purport to address. *See id.* at 1:16-27. In other words, the solution that the Sicard Patent purports to provide requires that the first and second metal conductors be part of the final metal layers and not some additional layer on top (which would only add cost and complexity that the Sicard Patent is trying to reduce).

It is thus not surprising that Infineon's expert Dr. Schaper agrees that this second metal layer containing the long final metal interconnects is the "final metal layer" of the chip to which the invention is directed. *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 92:14-93:25 ("Sicard is doing something to overcome the resistance of the…second layer of metal on the chip. That's the one that's got the long interconnects on it…That's the ones that he's concerned about, because those are the long interconnects that are in that—what to him is the final metal layer."). Sicard's purported invention is directed to minimize the resistance associated with this layer by shortening the distance that current must travel along the thin on-chip final metal layer before reaching the thick lead frame. *See id.* at 78:22-79:10 ("And Sicard's invention is how to minimize [the

resistance of the metal interconnects] by getting the current out of the thin conductors on-chip and getting it into this thick lead frame off-chip."), *see also* Sicard Patent at 3:49-54; 4:40-44. Connecting the frame to any piece of metal (as Infineon suggests) would not achieve this goal.

All told, the intrinsic record—the connections required by the text of Claim 1 of the patent, the description of metal conductors throughout the specification, and the objectives of the patent—all consistently and overwhelmingly support Volterra's construction that the first and second metal conductors must be parts of the final metal layer of the device. In contrast, and as discussed below, the metal conductors cannot be, as Infineon suggests, some sort of nebulous metal conductor of any shape, size, location, or composition divorced from the context of Sicard.

2. Infineon's Overbroad Construction Is Wholly Unsupported By The Patent And Represents A Legally-Improper Approach Designed To Engulf Undisclosed Interface Layers In The Accused Products

Infineon's proposal that the claimed first and second metal conductors can be any shape, in any location, and "any metal that permits an electric current to flow" is fundamentally divorced from the patent and the problem that it purports to solve. Instead, Infineon relies on non-technical dictionary definitions of "conductor" in support of its construction. D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi Reb. Decl.] ¶ 23. Sicard, however, is addressing specific types of conductors: the final metal that has an associated size and thinness that detrimentally affects the current capacity of the device. Sicard Patent at 2:35-42; Davis Decl., Ex. C [Schaper Dep. Tr.] at 192:5-14 ("The resistance he's talking about is the resistance caused by these long final metal interconnects, which is a detriment."). Infineon's reliance on a broad definition to the exclusion of Sicard's disclosure as a whole is improper. *See Phillips*, 415 F.3d at 1319 ("In sum, extrinsic evidence may be useful to the court, but it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence.").

The reason Infineon seeks to ignore the specification and broaden the claimed first and second metal layers beyond the disclosed final metal layer is clear. The accused Volterra products have a standard aluminum final metal layer and bumps that are made of solder. But, because of certain metallurgical properties of aluminum and solder, solder cannot form a "metallurgical bond" with aluminum. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 50.

Thus, the final metal layer in the accused products is not in contact with the accused bumps—taking them decidedly outside the scope of the Sicard Patent's claims. Unable to reconcile the structure of the accused products with the claims of the Sicard Patent, Infineon seeks to read the first and second metal conductors as any metal that conducts so that it can pursue an infringement theory that captures undisclosed, unclaimed external interface layers on top of the final metal layer on the chip (such as the under bump metallization (UBM) layer and the redistribution layer (RDL)). Not only are such interface layers above the final metal layer not disclosed in the patent, but additional metal layers deposited above the final metal layer are, in fact, disclaimed.[6]

There is no suggestion in the patent that the first and second metal conductors can be an additional layer outside the metal interconnect layers of the semiconductor device. The patent teaches that the invention is achieved **without the use** of a criticized additional layer deposited on top of the final metal layer. Sicard Patent at 1:48-58, 4:67-5:3. In fact, "the additional deposition step of this solution increases the complexity and cycle time of the manufacturing process which adds significant cost to the integrated power device." *Id.* at 1:52-55; *see also* 4:67-5:3 ("Moreover, the present invention does not require an expensive third thick metal deposition process as used in the prior art arrangement mentioned in the introduction.").

Infineon does not dispute these disclosures. Instead, it challenges whether the statements in Sicard amount to an explicit disclaimer of an additional metal layer above the final metal layer under *Thorner v. Sony Computer Ent't. Am. LLC*, 669 F.3d 1362 (Fed. Cir. 2012). This argument misses the mark at multiple levels.

At the outset, the law is clear that the specification and its disclosure of what the inventors purport to have invented is a touchstone of any proper claim construction analysis. *Phillips*, 415 F.3d at 1315 ("[T]he specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term."). Thus,

[6] Infineon's other criticisms of Volterra's construction are not relevant to the present dispute and distract from the core issue of whether an interface layer is covered under the claims. For example, Infineon argues that the first and second metal conductors should not be limited to a layer and that they do not need to be part of the same layer. These configurations are not relevant to the disputed issues and are merely a distraction.

even if Infineon were correct that the disclosure of the patent does not include an "explicit disclaimer," the overwhelming weight of the patents' disclosure (including the problems it purports to solve and the solution it claims to have invented) teach that the first and second metal conductors are part of the final metal layer and cannot capture any and all metals that conduct, let alone interface layers that sit above the final metal layer.

Moreover, even if Infineon were right that the proper claim construction requires a disclaimer (it does not), one skilled in the art would have understood the Sicard disclosure disclaiming what Infineon now seeks to cover. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 37-38. Unlike in *Thorner*, the Sicard Patent "repeatedly, consistently, and exclusively" excludes uses an additional metal layer above the final metal layer **and simultaneously disparages such an embodiment.** *Compare Thorner*, 669 F.3d at 1367 (finding that, without more, a showing that all examples of "attached" in the specification had attachments to the exterior surface of a human interface device was not enough to redefine "attached" to mean only "attached to an outer surface") *with In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1149-50 (Fed. Cir. 2012) (holding that the district court's conclusion that the claimed electrochemical sensor could not have external wires was supported by: (1) "every embodiment disclosed in the specification shows ... [a] sensor without external cables or wires," and (2) the discussion of the prior art in the specification identified external cables or wires as a deficiency in the prior art).

In such a case, the specification may give meaning to claim terms by implication even without an explicit disclaimer of claim scope. *See Abbott*, 696 F.3d at 1149-50. That is precisely the situation here. In Sicard, the specification repeatedly describes the bumps as being "in contact with" the final metal layer. Sicard Patent at Abstract, 2:48-52, 4:7-14. None of the embodiments teach or even hint at permitting an interface layer between the final metal layer and the bump. *See Id.* at Figs. 6, 7, 4:15-29.[7] And, similar to the patent in *Abbott* and in contrast to the patent in

[7] Infineon relies on *Epistar* for the argument that "'teaching against a technique' is not the same as disclaiming it." *See* D.I. 300 [Opening Br.] at 9-10 (citing *Epistar Corp. v. Int'l Trade Comm'n*, 566 F.3d 1321, 1335 (Fed. Cir. 2009)). However, in *Epistar*, there was only a "single, passing reference to [indium-tin oxide (ITO)] as a relatively unsatisfactory transparent electrical contact in the specification." *Id.* at 1336. Here, the goal of the purported invention is to avoid issues with the prior art, which it states is not necessary to practice the invention.

Thorner, the prior art solution using an additional layer above the final metal layer was disparaged as having associated problems that Sicard is designed to mitigate, and which the claimed invention renders unnecessary to practice the invention.

Unable to meaningfully confront that fact, Infineon tries to redirect the argument towards the different function between the prior art copper layer and the interface layers (e.g., the UBM and RDL) in the accused products. D.I. 300 [Opening Br.] at 11:12-22. However, the objective of the present invention is to mitigate the manufacturing difficulty, cost, and cycle time that the additional deposition step creates irrespective of the function of the copper layer. Sicard Patent at 1:52-58. But both experts agree that these interface layers that sit on top of the final layer are typically composed of multiple additional deposition steps—thus increasing the very manufacturing difficulty, cost and cycle time issues that Sicard seeks to avoid. D.I. 301-3 Baxter Decl., Ex. 3 [Schaper Op. Decl.] ¶¶ 96-97; D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 37-38; Davis Decl., Ex. C [Schaper Dep. Tr.] at 180:19-181:14. It is for these same reasons that Judge Spero previously held that a UBM interface layer is not disclosed and is in fact **taught away from** in Sicard. *See* Davis Decl., Ex. B [SJ Order] at 70-72. This evidence leaves no doubt that the first metal conductors and second metal conductors are parts of the final metal layer of the chip and cannot be expanded to additional interface layers above the final metal layer.

Additionally, the interface layers Infineon seeks to encompass within the scope of the first and second metal conductors are not subsequently developed technologies that were unknown at the time of Sicard. Both experts agree that interface layer technology (including the thick copper metal layer criticized in Sicard and the UBM and RDL layers in the accused products) were known at the time of the patent was filed. D.I. 300 [Opening Br.] at 8:19-9:11; s*ee* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 34-35; *see also* D.I. 301-3 Baxter Decl., Ex. 3 [Schaper Reb. Decl.] ¶ 19. Both experts also agree that the invention in Sicard neither discloses nor needs an interface layer. S*ee* Davis Decl., Ex. C [Schaper Dep. Tr.] at 169:8-170:12; *see also* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 34, 50. Had the Sicard Patent wished to disclose an additional metal layer or interface layer above the final metal layer, it could have done so. The language of the claims, the description of the invention, and the objectives of Sicard

make clear that that was not the intent or the invention—the first and second metal conductors are parts of the final metal layer of the chip and not an additional interface layer on top.

B. "bump" (Claims 1-8)

Claim Term	Infineon's Proposed Construction	Volterra's Proposed Construction
"bump"	raised metal contact	A raised metal structure formed partially on the final metal layer through an opening of a passivation layer

The parties dispute: (1) whether the claimed bumps can be formed on a metal other than the final metal layer; and (2) whether the bump can be a structure that is not disclosed in the patent. Again, Infineon's proposes to read the term bump in a vacuum based on a legally-improper, results-driven approach that ignores the teachings of the patent and the understanding of one of skill in the art. *See Medrad*, 401 F.3d at 1319.

1. Volterra's Proposed Construction Is Consistent With The Stated Objectives Of The Patent

The claims require a device in which bumps are formed in contact with the first and second metal conductors. Sicard Patent at Claim 1 ("each of the plurality of [first/second] metal conductors having **at least one bump in contact** therewith"), Claim 4 ("plurality of first metal conductors **have a plurality of bumps in contact therewith** and wherein each of the plurality of second metal conductors **have a plurality of bumps in contact therewith**").

The specification teaches the same requirement—that the bumps are formed in contact with the metal conductors, which are described exclusively as the second (final) metal layer in the preferred embodiments. *Id.* at Abstract ("[O]ne or more **bumps (8) formed in contact with the metal conductor (6).")**; 2:48-52 ("For each of the drain 4 and source 6 metal conductors, **one or more bumps 8 are formed in contact therewith.** Each bump 8 is formed of a metal, such as copper, or an alloy, such as an alloy of copper, tin and lead."; 4:20-22 ("A **second metal layer is deposited** on the second oxide layer 40 **to from** the metal conductor 34."); 4:7-14 ("FIG. 6 is a cross-sectional view of part of a LDMOS transistor die in accordance with the present invention showing one of the **bumps 8 in contact with a metal conductor 34** coupled to semiconductor regions 30."; *see also id.* at Figs. 6, 7).

Furthermore, the bumps of the present invention are described as "**bonded to** the source

of heat on the active face of the device." *Id*. at 5:4-7 ("**the present invention** allows for more efficient heat dissipation through the short, relatively large area (compared to wire bonding) **bumps bonded directly to the sources of heat on the active face of the device**"). As Infineon's expert Dr. Schaper testified, the source of heat on the active face of the device are the "on-chip interconnects," which in Sicard is also the "final metal layer." *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 147:1-8 ("Q. – when it says 'the bumps are bonded directly to the source of heat on the active face of the device,' that's referring to the bumps being attached to what's marked as item 34. Is that correct? A. Yeah. Item 34. And then through the other metal, down to the transistors. And that's where the – that's where the heat flow is.") (referring to item 34 in Fig. 6, which is the final metal layer in Sicard).

The bumps which are in contact with the metal conductors are the same bumps which are bonded to the source of heat on the active side of the device. Both experts also agree that the phrase "in contact with," requires **at least** that the bumps are in direct physical contact with the [first/second] metal conductors. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 43; Davis Decl., Ex. C [Schaper Dep. Tr.] at 150:1-12 (testifying "[c]ertainly physical contact is required but may not be enough" and that "it's important that you have contact, not just at a point, but over an area in order to carry the current"). The specification is thus consistent and exclusive in requiring that the bumps of the present invention are formed at least partially on the final metal layer.

The bumps must also be formed through an opening of the passivation layer (a non-metal protective layer placed above the final metal layer) to make that contact and bond:

> A passivation layer 44 is then formed over the second oxide layer 40 and part of the metal conductor 34 so as to provide an opening 46. **The bump 8 is then formed in the opening 46**. Preferably, the metal conductor 34 (extends a distance 48 of 2 microns above the second oxide layer 40 and the **bump 8 extends a distance 50 of 35 microns above the passivation layer 44.**

Sicard Patent at 4:23-28. It is undisputed that a passivation layer must be formed over the final metal layer to create the top surface of the semiconductor in order to protect the device from environmental damage (e.g., corrosion, scratches etc.). D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi

Reb. Decl.] ¶ 49; *see* Davis Decl., Ex. C [Schaper Dep. Tr.] at 39:21-40:24. The only way for a bump to contact the final metal layer is through an opening in the passivation layer. D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi Reb. Decl.] ¶ 49. This is exactly what Sicard discloses. *Id.*

2. Infineon's Proposed Construction Attempts To Improperly Expand The Scope Of The Claims To Cover The Accused Products Contradicts The Teachings Of The Patent

By broadening the scope of "bump" to be any raised metal contact, Infineon seeks to broaden the construction of bump to encompass the accused solder balls, which one of skill in the art would have understood are incapable of making the necessary contact with the final metal layer without an additional interface layer. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 50. Indeed, the claimed bump cannot encompass a solder ball because solder is incapable of contacting standard final metal layer to create the necessary "metallurgical bond" between the elements. *See* Sicard Patent at 4:30-37 (describing that "metallurgical bonds" must be formed both between the bump and the metal conductor and between the bump and the connection portions of the frame). This is because, as in the accused products, the final metal layer in standard semiconductor power devices was made of aluminum or an aluminum alloy. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 34; Davis Decl., Ex. C [Schaper Dep. Tr.] at 91:1-9. As a result, attaching solder bumps requires an interface layer above the final metal layer, which interface layer is inconsistent with the claimed invention of the patent as described in the preceding section. *Id.* at ¶ 38; *see* D.I. 301-3 Baxter Decl., Ex. 3 [Schaper Reb. Decl.] ¶¶ 19-21.

The described composition of the bumps further supports Volterra's construction that the bumps of the patent are formed at least partially on the final metal layer and through an opening in a passivation layer, rather than solder bumps on an interface layer. As Infineon's expert Dr. Schaper explained, there are some bumps that need an interface layer and some that do not. *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 169:8-170:12 ("And there's some kinds of bumps that do not require UBM."); *see also* Davis Decl., Ex. D [Volterra Action Schaper Dep. Tr.] at 198:7-199:12 ("Sicard does not have under-bump metallurgy. He has a different kind of bump."). The disclosed bumps would not need an interface layer because the type of bumps in Sicard (which are not solder balls) would be suitable for attaching to the typical standard metal layer without an

interface. Sicard Patent at 2:50-52; *see also* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 49-50 (copper bumps, and alloys of copper, tin and lead can be formed directly in contact with the final metal layer, whether it is a standard aluminum layer or some other atypical metal such as copper, without an interface layer).

3. Infineon Has Failed To Raise Any Meaningful Objection To Volterra's Construction

Infineon misconstrues Volterra's construction as limited to the embodiments in Figs. 6 and 7. Although Figs. 6 and 7 disclose a typical bump, Volterra does not contend that under its construction the bump must be formed partially on the final metal layer and partially on the passivation layer as Infineon alleges. D.I. 300 [Opening Br.] at 14:18-20. Volterra's construction does not rule out a bump that is only in contact with the final metal layer. *See* D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi Reb. Decl.] ¶ 55. However, no such embodiment is in dispute.

Infineon has consequently failed to raise any meaningful objection to Volterra's construction. This is unsurprising given that only Volterra's construction captures what is compelled by the plain language of "bumps" in light of the claim language, the specification, and the objectives of the patent. Infineon's overbroad construction should be rejected as another attempt to ignore the teachings of the patent and claim undisclosed and entirely unsupported features of the accused products, and should be rejected as such.

C. "frame" and "connection portions" (Claims 1-8)

Claim Term	Infineon's Proposed Construction	Volterra's Proposed Construction
"frame"	lead frame	a support structure that includes connection portions for connecting to the bumps and other portions for connecting to a PCB
"connection portions"	parts of the frame that extend across at least a portion of the die and are spaced apart from one another	portions of the frame for connecting to the bumps

The parties' dispute centers around whether the "frame" encompasses a lead frame consisting only of the plurality of first and second connection portions (Infineon's position) or whether the frame includes the connection portions and other portions (Volterra's position). At the heart of this dispute is Infineon's apparent view that the "frame" can be a collection of isolated metal strips, notwithstanding the necessary characteristics of the lead frame as known to

individuals of ordinary skill in the art at the time of the patent and the Sicard Patent's own description of a lead frame.

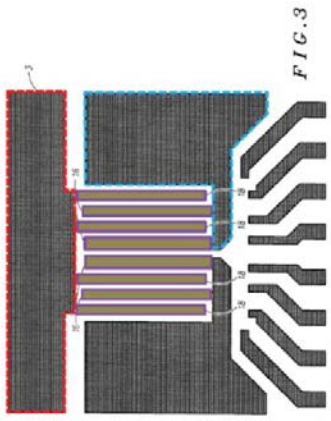
1. Volterra's Proposed Construction Describes The Essential Features Of A Lead Frame Consistent With The Claims And Specification

The claims and the specification make clear that there are two parts to the frame in Sicard: (1) portions of the frame for connecting to the bumps (the "connection portions"); and (2) other portions that provide the external connections of the device to a PCB. Claim 1 requires that the frame include first and second "connection portions" **and** provide external connections to the semiconductor regions of the device:

> a frame formed of high conductivity material, the frame comprising a plurality of first connection portions for connecting to the at least one bumps of the first metal conductors and a plurality of second connection portions for connecting to the at least one bumps of the second metal conductors, ***the frame providing external connections to the semiconductor regions of the device***.

Sicard Patent at Claim 1. These external connections are provided to the external wiring of the product level circuit board (*e.g.*, PCB) by the "other portions" of the frame.

The specification also supports Volterra's construction. Each of the patent's depictions of the "frame"—in "accordance with the present invention"—show "other portions" connected to the connection portions. *Id.* at Figs. 2, 3. Figure 3 is described as "an example of a **whole frame 3 in accordance with an embodiment of the present invention.**" *Id.* at 3:20-22. Marked up Figure 3 below makes clear that there are "other portions" of the frame, outlined in blue and red, which are distinct from, but connected to, the "connection portions" 16 and 18. *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 134:4-21; D.I. 301-5 Baxter Decl. Ex. 5 [Szepesi Reb. Decl.] ¶ 82 ("The 'connection portions' are marked with semi-transparent yellow filling color with purple outline. As Fig. 3 clearly shows the whole frame is significantly more than these 'connection portions.' Two of those 'other portions' are indicated with red and blue dotted line marking around their edges. The marked 'other portions' do not



constitute all the 'other portions' of the whole frame.")

The connection portions and the other portions are shown in both the "whole frame" and in "part of the frame" shown in Fig. 2. Sicard Patent at 2:15-17 ("Fig. 2 is a top plan view of **part of a frame** of a LDMOS transistor device in accordance with the present invention"), 2:18-19 ("Fig. 3 is a top plan view of a **whole frame** of a LDMOS transistor device in accordance with the present invention."). Dr. Schaper argues that these disclosed other portions of the frame in every embodiment "could be" unnecessary. *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 136:25-137:21. However, there is nothing in the intrinsic record that teaches or hints that the other portions are optional or that the frame could be composed only of isolated connection portions that provide connection to external circuitry (*e.g.* on a PCB). *See* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 68. Additionally, Dr. Schaper has not offered **any** prior art to support his contention that lead frames could be a collection of isolated connection portions.

Importantly, it is these "other portions" of the frame that allow the present invention to connect the semiconductor regions, through the connection portions, to a printed circuit board ("PCB") enabling the connection of the power device to external components on the PCB.[8]

> As mentioned above, preferably the frame is formed of a thick metal which, **through the connecting portions**, are used to form the metal interconnections to the device semiconductor regions.

Sicard Patent at 4:38-41.

> The **present** invention also allows for more efficient heat dissipation through the short, relatively large area (compared to wire bonding) bumps bonded directly to the sources of the heat on the active face of the device, through the metal intensive connecting portions of the frame **to the product level printed circuit board**.

Id. at 5:4-9. These disclosures confirm that the other portions of the frame are the only portions disclosed that can operate to implement a necessary functionality of the frame as claimed, *i.e.*

[8] Volterra's construction does not **require** that the frame be connected to a PCB, rather it must have "other portions **for connecting to** a PCB." As a person of ordinary skill would have known, semiconductor power devices in themselves are not very useful. D.I. 301-5 Baxter Decl., Ex. 5 [Szepesi Reb. Decl.] ¶ 86. They function when they are connected to external wiring, which would have typically been on a PCB. *Id.* Regardless, Infineon's argument that the power semiconductor device could be connected to other things like a substrate is a red herring because the ultimate destination with the external wiring is not in dispute.

connecting the "connection portions" to a PCB. *Id.*

Moreover, these other portions of the lead frame are necessary to provide support for the power semiconductor device as well as to provide external connections. *Id.* 3:17-20 ("In addition, to providing connections to the semiconductor regions of the device, the frame also is the lead frame of the device **and so provides a support for the LDMOS transistor die.**"). The connection portions would not be understood, nor are they described, as providing support for the chip (transistor die) and providing external connections. *See* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 58. Rather, consistent with Volterra's construction, the frame requires both "connection portions for connecting to the die," as well as these robust "other portions" to provide support for the device and make connections to external circuitry.[9]

2. Infineon's Objection To Volterra's Proposed Construction Is Belied By Its Own Construction

Infineon argues that there is "no intrinsic evidence showing that the patentees redefined the term 'frame' by lexicography or disclaimer," and yet **Infineon ignores its own construction** that the frame has the characteristics of a "lead frame." D.I. 300 [Opening Br.] at 18:13-16. Both parties agree that what is disclosed in Sicard is a lead frame. *See id.* at 16:19-24. Volterra's construction simply includes the essential parts of a lead frame that are also the subject of a dispute. Perhaps realizing that—consistent with Volterra's proposed construction—the "lead frame" as described in the claims, the specification, and as understood by those of ordinary skill in the art would include both "connection portions" and the rest of the "frame," Infineon is now trying to ignore the structure of a "lead frame." Rather, Infineon seeks a construction of frame to include a collection of disconnected portions of metal, which would be contrary to the knowledge of one skilled in the art and every preferred embodiment in the patent.

3. Infineon's Proposed Construction Appears To Read Out Every

[9] As described in the patent, the frame extends over the chip. Sicard Patent at 3:13-17. Even Dr. Schaper acknowledges that, because the connection portions are only "two hairs wide," the bonding process "would deform the connection portion when you make the first bond." Davis Decl. Ex. C [Schaper Dep. Tr.] at 70:7-71:23. By comparison, as Dr. Schaper explains, the areas of copper which are not the connection portions (the other portions of the frame) are "fairly robust" and enable "soldering to the board using normal surface mount solder paste deposits." D.I. 301-3 Baxter Decl. Ex. 3 [Schaper Reb. Decl.] ¶ 46.

Disclosed Embodiment Of The Frame

Infineon's claim construction of "connection portions" purports to cover parts of the frame that are "spaced apart from one another," apparently intending to read the frame on a collection of disconnected metal strips.[10] Such an interpretation would improperly exclude every disclosed embodiment of the "connection portions." *SynQor, Inc. v. Artesyn Tech., Inc.*, 709 F.3d 1365, 1378-79 (Fed. Cir. 2013) (noting that a claim construction that excludes the preferred embodiment is rarely, if ever, correct and would require highly persuasive evidentiary support). In both Figs. 2 and 3, each "connection portion" of the frame is not completely spaced apart from one another because a plurality of the "first connection portions" and a plurality of the "second connection portions" of the frame are electrically connected to one another by additional, other portions of the frame—just as Volterra's construction proposes. Sicard Patent at Figs. 2, 3.

Because Infineon's construction of connection portions does nothing to address the actual controversy and would only confuse the jury, it must be rejected. Volterra's construction in contrast clarifies that there are connection portions for connecting to the bumps, consistent with the descriptions in the claims and the specification.

D. "interdigitated" (Claim 4)

Claim Term	Infineon's Proposed Construction	Volterra's Proposed Construction
"interdigitated"	alternately arranged in adjacent rows	structures of interlocking fingers

[10] If Infineon proposes a different definition, it is unclear what scope is intended by the "spaced apart" portion of its construction. Infineon suggests that this portion of its construction is necessary in light of Volterra's invalidity contentions. But as pointed out by Dr. Szepesi, Infineon misinterprets Volterra's contentions for the JP 5-235086 prior art reference, purporting to address a controversy that does not exist. D.I. 301-13 Baxter Decl., Ex. 13 [JP 5-235086]; *See* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 69-72. Infineon alleges that "Volterra appears to take the position that the single lead 23 can be divided into a plurality of separate connection portions based on the location of the electrode pads 25." D.I. 300 [Opening Br.] at 20:23-25. At no point has Volterra made such a suggestion. Rather, as Volterra's invalidity contentions make clear, it is not alleging that a single lead (an electrode pad region) would be multiple connection portions. *See* D.I. 301-15 Baxter Decl., Ex. 15 [App'x A-2 to Volterra's Invalidity Contentions]. As Volterra described, this reference discloses that there may be a **plurality** of electrode pad **regions**. *See* D.I. 301-14 Baxter Decl., Ex. 14 [JP 5-235086 Translation] ¶ 20 ("This is a diagram wherein the dispersed **electrode pad section is disposed in just one row** parallel to the periphery of the semiconductor chip (20), but depending on the surface area of the power MOS transistors (1 , 2, 3, 4), **there could be a plurality of rows**. Note that (24) is a lead for the control circuit section (5)."). The electrode pad **regions** are leads containing a plurality of individual electrode pads. *See id.* Thus, there is no need for the "spaced apart" requirement, let alone support for Infineon's apparent interpretation of that language.

The parties agree that the specification uses the term "interdigitated" and "alternating" interchangeably. D.I. 300 [Opening Br.] at 22:13-14, 22:20-21; Sicard Patent at 2:46-62. This is what is meant by Volterra's construction—that the "plurality of first metal conductors" are alternating with the "plurality of second metal conductors." Infineon, on the other hand, goes beyond the disclosure in the specification by adding the term also requires that the items that are interdigitated with each other are "arranged in adjacent rows."

The only support that Infineon has identified for this additional requirement is the depiction of the preferred embodiment shown in Figure 1. D.I. 300 [Opening Br.] at 22:22-23. But neither the claim language nor the specification requires that each first metal conductor be in a row immediately adjacent to a second metal conductor without anything between. To the contrary, such a requirement is improper as it would read out the requirement in dependent Claim 3 that the conductors are arranged in parallel. Sicard Patent at Claim 3 ("…wherein each of the plurality of first and second metal conductors are arranged in parallel extending in a first direction."); *see Cat Tech. LLC v. TubeMaster, Inc.*, 528 F.3d 871, 885 (Fed. Cir. 2008) (declining to adopt a claim construction that would render a claim limitation meaningless).

E. "bumps on the first metal conductors are substantially aligned in first lines which extend in a second direction" and "bumps on the second metal conductors are substantially aligned in second lines which extend in the second direction" (Claims 5-8)

Claim Term	Infineon's Proposed Construction	Volterra's Proposed Construction
"bumps on the first metal conductors are substantially aligned in first lines which extend in a second direction" "bumps on the second metal conductors are substantially aligned in second lines which extend in the second direction"	plain and ordinary meaning, except for "bumps" as addressed separately in this chart	two-dimensional pattern of bumps where bumps to be connected to the frame are aligned in a direction different from the first direction

There are two primary disputes between the parties: (1) whether bumps can be arranged in first and second directions that are the same (Infineon's position) or should be different directions (Volterra's contentions); and (2) whether bumps actually have to be arranged in particular directions (Volterra's) or whether Infineon can simply draw *ad hoc* (and *post hoc*) lines through

an array of bumps to select a first direction and a second direction at will (Infineon's position). *See* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 81.

1. The "First Direction" And "Second Direction" Are Different

Based on the intrinsic record, the first direction must be different from the second direction. *See* D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶¶ 72-76; Sicard Patent at Claim 5, 3:29-43; *see id.* at Figs. 1, 4.

Claim 1 requires that there be a "plurality of first connection portions for connecting to the at least one bumps of the first metal conductors and a plurality of second connection portions for connecting to the at least one bumps of the second metal conductors." *Id.* at Claim 1. However, Claim 1 does not require that the "at least one bumps" on the plurality of first and second metal conductors have any specific arrangement, so long as the bumps can be connected to the connection portions of the frame. *Id.* at Claim 1. The bumps could be arranged in any of the disclosed embodiments: "randomly" such that there is no second direction (*see id.* at Fig. 5, 3:57-62), extending in a second direction perpendicular to the conductors (*see id.* at Fig. 1, 3:30-37), or extending in a second direction skewed to the conductors (*see id.* at Fig. 4, 3:38-43).

Claim 5 is dependent on Claim 1. *Id.* at Claim 5 ("A semiconductor power device according to claim 1…"). Claim 5 narrows the connections to those in which the arrangement of bumps is not just in the same direction as the conductors (Fig. 5), but extends in a different direction (Figs. 1, 4) in alignment with the connection portions. *See id.* at Claims 1, 5. Claim 5 is therefore directed to the embodiments in which the bumps are arranged in a two-dimensional pattern (aligned in one direction and extending in a different direction) such that the first and second connection portions of the frame are attached to the bumps in a direction different than the direction of the first and second metal conductors.

2. The Arrangement Of Bumps Is With Respect to the Connection Portions Not A Post Hoc Line Drawing Exercise

Tracking the language of the claims, the specification discloses (consistent with Volterra's construction) that the bumps are arranged such that they are "aligned in the first 10 and second 12 lines respectively, which lines extend in a second direction Y." *Id.* at 3:8-11, 3:31-36, 3:38-42; *see id.* at Figs. 1, 4. The first and second lines in the Y direction correspond to the direction along which the respective pluralities of first and second connection portions of the frame connect to the bumps. *Id.* at 3:44-47. Sicard also discloses that the arrangement (separation) of the bumps is tied to the connection portions. *Id.* at 3:8-11 ("The particular number and arrangement of the connecting portions of the frame depend on the number of metal conductors, the number of bumps on each metal conductor and the spatial arrangement of the bumps.")). Marked up Fig. 1 below shows the two-dimensional pattern of bumps described in the specification and mapping to Claim 5, which is described in Sicard as "a spatial arrangement of bumps." *Id.* at 3:8-11.

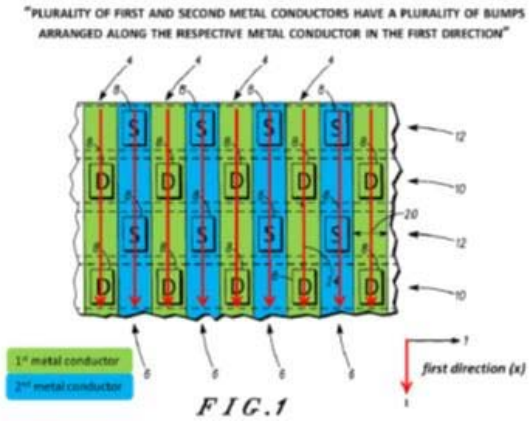


FIG.1

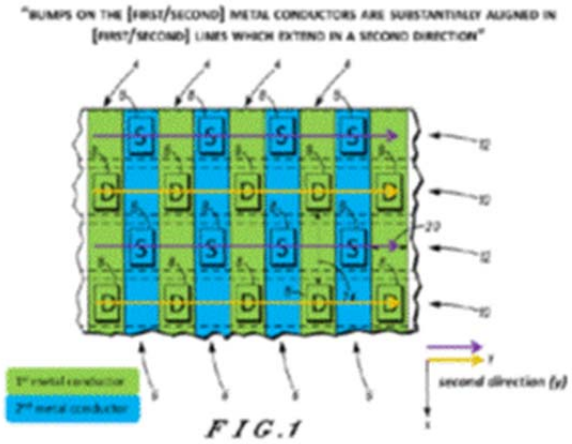
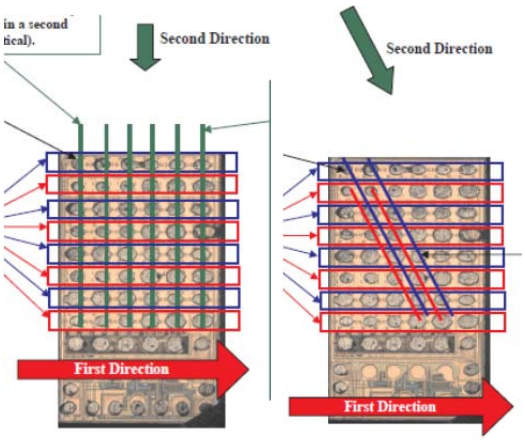


FIG.1

This is further consistent with the plain language of Claim 5 which requires the bumps of the first metal conductors be aligned in separate and distinct lines, *i.e.* the plurality of bumps on the first metal conductors aligned in "**first** lines" and the plurality of bumps on the second metal conductors aligned in "**second** lines." *Id.* at Claim 5. As a person of ordinary skill in the art would have understood, Sicard distinguishes between "first lines" and "second lines" **because** bumps that are to be attached to the connection portions cannot be any bumps along a line. D.I. 301-4 Baxter Decl., Ex. 4 [Szepesi Op. Decl.] ¶ 82. Specifically, bumps associated with the "first metal conductors" cannot be connected to bumps associated with the "second metal conductors" because this would short circuit the "first" and "second semiconductor regions" of the device and render it nonfunctional.

Id. Therefore, the plurality of bumps arranged on the first metal conductors must be arranged such that the **first** lines of bumps extending in a second direction only include bumps of the same type (*e.g.*, bumps in contact with the first metal conductors only) to enable connecting of the connection portions in the second direction. *Id.* This is also true for the bumps arranged on the second metal conductors arranged in second lines of bumps extending in the second direction. *Id.*

On the other hand, Infineon interprets the claim to simply require an *ad hoc* (and *post hoc*) line drawing exercise that fails to give any meaning to the claim. Infineon goes so far as to allege that the exact same arrangement of bumps can be aligned in lines which extend in multiple second directions depending on how Infineon and its counsel choose to draw those lines. *See, e.g.*, Davis Decl., Ex. I [Infineon's 4th Amended Infr. Cont. App. A] at 62, 64. Such an interpretation is in direct contrast with the description in the specification and the plain language of the claim.



3. Infineon's Proposed Interpretation Is Inconsistent With The Claim Language And Specification

Once again, Infineon offers a construction in a vacuum. Although the words "direction" and "lines" are ordinary terms, they are used to describe a particular arrangement of bumps. D.I. 300 [Opening Br.] at 23:15-16. The requirements for that arrangement are disputed and thus must be resolved in claim construction. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1361-62 (Fed. Cir. 2008) ("In this case, the 'ordinary' meaning of a term does not resolve the parties' dispute, and claim construction requires the court to determine what claim scope is appropriate in the context of the patents-in-suit. This court has construed other 'ordinary' words for these and other related reasons.").

Infineon first argues that "neither the claim language nor the specification supports a requirement that the second direction is a 'direction different from the first direction.'" D.I. 300 [Opening Br.] at 24:7-25. However, if the first and second direction can be the same direction,

then the "plurality of bumps on the [first/second] metal conductors" are **always** aligned in a second direction. This would render the term "extending in a second direction" meaningless. *Id.* at 23:7-8; *see Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006) (claims must be "interpreted with an eye toward giving effect to all terms in the claim").

Next, Infineon argues the Sicard specification discloses alternative embodiments wherein the connection portions extend in the same direction as the metal conductors. *See* Sicard Patent at Fig 5, 3:57-65. This is not disputed. But, the mere fact that there are alternative embodiments disclosed in the Sicard Patent does not change the language of the claim where it is directed to other embodiments also described in the intrinsic evidence. *August Tech. Corp. v. Camtek, Ltd.*, 655 F.3d 1278, 1285 (Fed. Cir. 2011) ("The mere fact that there is an alternative embodiment disclosed in the [asserted patent] that is not encompassed by [our] claim construction does not outweigh the language of the claim, especially when the court's construction is supported by the intrinsic evidence.") (*citing TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008)). Here, the description of alternative single-direction embodiments in the specification plainly falls outside the claim because they would not have the required second direction. *See* Sicard Patent at 3:57-65.[11] Thus, read in the context of the specification, Claim 5 of the patent does not encompass the alternative embodiments where the connection portions connect to the bumps in the same direction as the metal conductors.[12]

Infineon also asserts that "Claim 5 does not mention the connection portions or the frame at all." D.I. 300 [Opening Br.] at 25:7-8. However, Infineon ignores that Claim 5 is dependent on Claim 1, which requires a frame with connection portions for connecting to bumps. Sicard Patent Claim 1. The only construction that then gives meaning to the entirety of the claims as a whole is that the "bumps on the [first/second] metal conductors are substantially aligned in [first/second] lines which extend in a second direction" are arranged in a two-dimensional pattern of bumps

[11] Infineon's expert Dr. Schaper acknowledged that, unlike the preferred embodiments in Figs. 1 and 4, Fig. 5 is neither described as having a second direction nor depicts having a second direction. *See* Davis Decl., Ex. C [Schaper Dep. Tr.] at 202:16-203:1, 205:11-18, 207:7-15.

[12] Instead, these embodiments are encompassed by Claim 1 of the patent.

where bumps to be connected to the frame are aligned in a direction different from the first direction of bumps aligned on the respective conductor.

4. Volterra's Proposed Construction Is The Only Construction Which Comports With The Doctrine Of Claim Differentiation

The doctrine of claim differentiation does not "counsel against" Volterra's construction, as Infineon suggests, but rather reinforces it. D.I. 300 [Opening Br.] at 24:14-25, 25:12-22. Claim 7 requires that the second direction is **skewed** to the first direction. Contrary to Infineon's proposal that "'skewed' means not parallel," the term skewed in the context of the patent means a direction different than the first but not perpendicular. *See id.* at fn. 11; *see also* Davis Decl., Ex. E [Merriam Webster 1998 "skew"] ("skew" is defined as "set, placed, or running obliquely"); *see also* Davis Decl., Ex. F [Merriam Webster 1998 "oblique"] ("oblique" is defined as "neither perpendicular nor parallel"). Rather, consistent with Volterra's construction, Claim 5 is broader than Claim 6 and Claim 7 because it encompasses all embodiments where the first direction is different than the second direction (*e.g.*, substantially perpendicular (claim 6) or skewed (at an angle neither perpendicular nor parallel) (claim 7)). *See AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1242 (Fed. Cir. 2003) ("Under the doctrine of claim differentiation, dependent claims are presumed to be of narrower scope than the independent claims from which they depend.").

Claim 9 is also narrower than Claim 5. Claim 9 narrows Claim 5 by requiring that "**each** of the [first/second] connection portions for connecting to the bumps arranged in a respective one of the [first/second] lines extending in a second direction." Claim 5 could cover embodiments where multiple lines of bumps are connected to a single connection portion because the first lines and second lines of bumps could be next to each other rather than alternating as in Claim 8.

In view of the above, Volterra's construction is the only construction which comports with the plain language of the claims, the embodiments of the patent, and the doctrine of claim differentiation and should be adopted.

Dated: April 24, 2014

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